The following claims are presented for examination:

1. (Original) An apparatus comprising:

a first NMOS field effect transistor having a gate terminal, a source terminal, and a drain terminal;

a first resistor having a first terminal and second terminal, wherein said first terminal of said first resistor is electrically connected to said gate terminal of said first NMOS field effect transistor;

a first PMOS field effect transistor having a gate terminal, a source terminal, and a drain terminal, wherein said source terminal of said first PMOS field effect transistor is electrically connected to said source terminal of said first NMOS field effect transistor, and wherein said drain terminal of said first PMOS field effect transistor is electrically connected to said source terminal of said first PMOS field effect transistor; and

a second NMOS field effect transistor having a gate terminal, a source terminal, and a drain terminal, wherein said drain terminal of said second NMOS field effect transistor is electrically connected to said drain terminal of said first PMOS field effect transistor.

2. (Original) The apparatus of claim 1 wherein a first voltage applied to said second terminal of said first resistor is greater than a second voltage applied to said drain terminal of said first NMOS field effect transistor by at least the gate-to-source threshold voltage of said first NMOS field effect transistor.

3. (Original) The apparatus of claim 1 further comprising a third NMOS field effect transistor having a gate terminal, a source terminal, and a drain terminal, wherein said drain terminal of said third NMOS field effect transistor is electrically connected to said source terminal of said second NMOS field effect transistor.

4. (Original) The apparatus of claim 3 wherein said source terminal of said third NMOS field effect transistor is electrically connected to ground voltage.

5. (Original) The apparatus of claim 3 further comprising a fourth NMOS field effect transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said fourth NMOS field effect transistor is electrically connected to said source terminal of said second NMOS field effect transistor.

6. (Original) The apparatus of claim 5 further comprising a second PMOS field effect transistor having a gate terminal, a drain terminal, and a source terminal, wherein said drain terminal of said second PMOS field effect transistor is electrically connected to

said drain terminal of said fourth NMOS field effect transistor, wherein said drain terminal of said second PMOS field effect transistor is electrically connected to said source terminal of said second PMOS field effect transistor, and wherein said gate terminal of said second PMOS field effect transistor is electrically connected to said gate terminal of said first PMOS field effect transistor.

7. (Original) The apparatus of claim 6 further comprising a fifth NMOS field effect transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said fifth NMOS field effect transistor is electrically connected to said source terminal of said second PMOS field effect transistor, and wherein said drain terminal of said fifth NMOS field effect transistor is electrically connected to said drain terminal of said first NMOS field effect transistor.

8. (Original) The apparatus of claim 7 further comprising a second resistor having a first and second terminal, wherein said first terminal of said second resistor is electrically connected to said gate terminal of said fifth NMOS field effect transistor, and wherein said second terminal of said second resistor is electrically connected to said second terminal of said first resistor.

9. (Original) The apparatus of claim 8 wherein the gate terminal of said first PMOS field effect transistor is connected to a control voltage in the range of about 0.9 Volts to about 1.3 Volts.

10. (Original) The apparatus of claim 8 wherein said first NMOS field effect transistor, said second NMOS field effect transistor, said third NMOS field effect transistor, said fourth NMOS field effect transistor, said fifth NMOS field effect transistor, said first PMOS field effect transistor, and said second PMOS field effect transistor are produced using a 0.18 micron process.

11. (Original) The apparatus of claim 8 wherein a supply voltage applied to said drain terminal of said first NMOS field effect transistor is about 1.8 volts.

12. (Original) The apparatus of claim 8 further comprising:

a positive input terminal wherein said positive input terminal is electrically connected to said gate terminal of said second NMOS field effect transistor;

a negative input terminal wherein said negative input terminal is electrically connected to said gate terminal of said fourth NMOS field effect transistor;

a bias input terminal wherein said bias input terminal is electrically connected to said gate terminal of said third NMOS field effect transistor;

a control input terminal wherein said control input terminal is electrically connected to said gate terminal of said first PMOS field effect transistor;

a positive output terminal wherein said positive output terminal is electrically connected to said source terminal of said fifth NMOS field effect transistor; and,

a negative output terminal wherein said negative out terminal is electrically connected to said source terminal of said first NMOS field effect transistor.